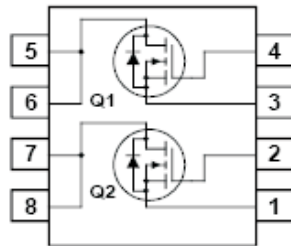
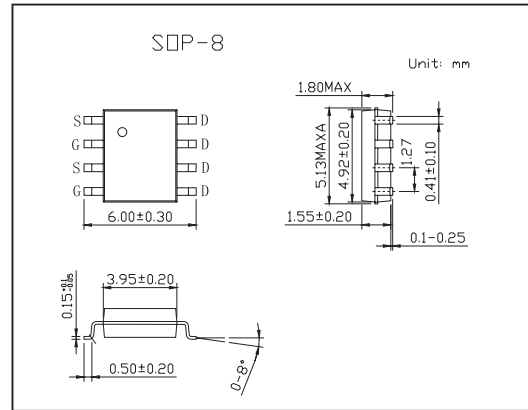


Dual N-Channel Logic Level PowerTrench MOSFET

KDS6910

■ Features

- 7.5 A, 30 V. $R_{DS(ON)} = 13\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
 $R_{DS(ON)} = 17\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- Low gate charge
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current Continuous (Note 1a)	I_D	7.5	A
Drain Current Pulsed		20	A
Power Dissipation for Single Operation (Note 1a)	P_D	1.6	W
Power Dissipation for Single Operation (Note 1b)		1	
Power Dissipation for Single Operation (Note 1c)		0.9	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78	$^\circ\text{C/W}$

KDS6910

■ Electrical Characteristics Ta = 25°C

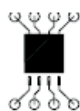
Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V, ID = 250 μ A	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BVDSS}{\Delta T_J}$	ID = 250 μ A, Referenced to 25°C		28		mV/°C
Zero Gate Voltage Drain Current	IDSS	VDS = 24 V, VGS = 0 V			1	μ A
		VDS = 24 V, VGS = 0 V, TJ = 55°C			10	
Gate-Body Leakage, Forward	IGSSF	VGS = 20 V, VDS = 0 V			100	nA
Gate-Body Leakage, Reverse	IGSSR	VGS = -20 V, VDS = 0 V			-100	nA
Gate Threshold Voltage	VGS(th)	VDS = VGS, ID = 250 μ A	1	1.8	3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta VGS(th)}{\Delta T_J}$	ID = 250 μ A, Referenced to 25°C		-4.7		mV/°C
Static Drain-Source On-Resistance	RDS(on)	VGS = 10 V, ID = 7.5 A		10.6	13	m Ω
		VGS = 4.5 V, ID = 6.5 A		13	17	
		VGS = 10 V, ID = 7.5 A, TJ = 125°C		14.5	20	
On-State Drain Current	ID(on)	VGS = 10 V, VDS = 5V	20			A
Forward Transconductance	gFS	VDS = 5 V, ID = 7.5A		36		S
Input Capacitance	Ciss	VDS = 15 V, VGS = 0 V, f = 1.0 MHz		1130		pF
Output Capacitance	Coss			300		pF
Reverse Transfer Capacitance	Crss			100		pF
Gate Resistance	RG	VGS = 15 mV, f = 1.0 MHz		2.4		Ω
Turn-On Delay Time	td(on)	VDD = 15 V, ID = 1 A, VGS = 10 V, RGEN = 6 Ω		9	18	ns
Turn-On Rise Time	tr			5	10	ns
Turn-Off Delay Time	td(off)			26	42	ns
Turn-Off Fall Time	tf			7	14	ns
Total Gate Charge at VGS=10V	Qg(TOT)				17	24
Total Gate Charge VGS=5V	Qg	VDS = 15 V, ID = 7.5 A (Note 2)		9	13	nC
Gate-Source Charge	Qgs			3.1		nC
Gate-Drain Charge	Qgd			2.7		nC
Maximum Continuous Drain-Source Diode Forward Current	IS				1.3	A
Drain-Source Diode Forward Voltage	VSD	VGS = 0 V, IS = 1.3 A (Not 2)			1.2	V
Diode Reverse Recovery Time	trr	IF = 7.5A		24		nS
Diode Reverse Recovery Charge	Qrr	diF/dt = 100 A/ μ s		13		nC

Notes:

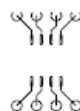
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%